FEATURES
Complete with High Accuracy Sample/Hold and
A/D Converter
Low Power Consumption: 650mW max, $V_S = \pm 15V$
Rated Performance: $-25^\circ C$ to $+85^\circ C$
Low Nonlinearity (DAS1158 and DAS1159)
  Differential: $\pm 0.0015\%$ FSR max
  Integral: $\pm 0.003\%$ FSR max
Differential T.C.: $\pm 1$ppm/$^\circ C$ max
High Throughput Rate: 18kHz min
Byte-Selectable Tri-State Buffered Outputs
Internal Gain & Offset Potentiometers
All Hermetically-Sealed Semiconductors
Improved Second Source to A/D/A/M-834 and
A/D/A/M-835 Modules

APPLICATIONS
Seismic Data Acquisition
Portable Field Instrumentation
Automated Test Equipment
Process Control Data Acquisition
Medical Instrumentation

GENERAL DESCRIPTION
The DAS1157/DAS1158/DAS1159 are 14-/15-/16-bit sampling
analog-to-digital converters. They are ideally suited for use in
portable and remote data acquisition equipment where low
power consumption (650mW maximum) and wide temperature
range ($-25^\circ C$ to $+85^\circ C$ rated performance) are required.
DAS1157/DAS1158/DAS1159 provide guaranteed high accuracy
and high stability system performance essential to medical,
analytical and process control equipment: differential nonlinearity
of $\pm 0.0015\%$ max and integral nonlinearity of $\pm 0.003\%$ max
(DAS1158 and DAS1159); no missing codes guaranteed; gain
T.C. of $\pm 8$ppm/$^\circ C$ max, zero T.C. of $\pm 80\mu V/$$^\circ C$max
and differential nonlinearity T.C. of $\pm 1$ppm/$^\circ C$max.
The wide dynamic range will enhance the performance of critical
measurements in gas and liquid chromatography, blood analyzers,
distributed data acquisition in factory automation and power
generating equipment, and in automatic test equipment.
The DAS1157/DAS1158/DAS1159 make use of Analog Devices'
proprietary CMOS technology to achieve low power operation,
while utilizing the latest integrated circuit and thin-film compo-
ments to achieve the highest level of performance and reliability.
All hermetically-sealed semiconductor components are used
to insure added reliability over a wide range of operating
conditions.

Figure 1. DAS1157/DAS1158/DAS1159 Block Diagram

As shown in Figure 1, each device contains a precision sample/hold
amplifier, high accuracy 14-/15-/16-bit analog-to-digital converter,
precision reference, CMOS tri-state output buffers (for direct 8-
bit or 16-bit bus interface), user accessible gain and offset adjust
potentiometers, and power supply bypass capacitors, all in a
compact low profile 2" x 4" x 0.375" metal case package. No
additional components are required for operation.
## SPECIFICATIONS

(typical @ +25°C, Vg = ±15V, Vb = +5V unless otherwise specified)

<table>
<thead>
<tr>
<th>MODEL</th>
<th>DAS1157</th>
<th>DAS1158</th>
<th>DAS1159</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESOLUTION</td>
<td>14 Bits</td>
<td>15 Bits</td>
<td>16 Bits</td>
</tr>
</tbody>
</table>

### DYNAMIC PERFORMANCE

- **Throughput Rate**: 1kHz max
- **S/H Acquisition Time**: 5µs max
- **S/H Aperture Delay**: 250ns
- **S/H Aperture Uncertainty**: ±80mV
- **Feedthrough Rejection**: ±90dB
- **Dropout Rate**: 0.001% FS max
- **Output Absorption Error**: ±0.005% of Input Voltage

### ACCURACY

- **Integral Nonlinearity**: ±0.005% FS max
- **Differential Nonlinearity**: ±0.005% FS max
- **No Missing Codes**: Guaranteed
- **±0.5 μA Noise (S/H Input A/D)**: 0.003% FS + 0.003% FS max

### STABILITY

- **Integral Nonlinearity T.C.**: ±2ppm/°C max
- **Input T.C.**: ±50μV/°C, ±50µV/°C max
- **Temperature Coefficient (T.C.)**: ±0.05%/°C
- **Power Supply Sensitivity**: ±0.005% FS/°C
- **Warm-Up Time**: Less than 1 minute

### ANALOG INPUT

- **Voltage Range**: 5V, >10V
- **Input Impedance**: 2.5MΩ ± 1%
- **S/H Input Impedance**: 100Ω/100µF

### DIGITAL INPUTS

- **A/D Trigger**: Positive or Negative, Edge Triggered
- **Logic Levels**: 4.096V CMOS Compatible
- **S/H Control**: Sample & Hold, TTL Compatible
- **Low-Eleven, Hold Enable**: Logic 0, CMOS/TTL Compatible

### DIGITAL OUTPUTS

- **Parallel Data Outputs**: Binary
- **Bipolar**: Offset Binary, Z-Complement
- **Output Driver**: 2 TTL Loads
- **End of Conversion**: Logic "1" during conversion
- **Output Drive**: 2 TTL Loads

### INTERNAL REFERENCE VOLTAGE

- **Output Voltage**: ±10V, ±0.1%

### POWER REQUIREMENTS

- **Supply Voltage**: 5V, ±10V
- **Operating Voltage**: ±12V
- **Power Supply Current**: 1mA
- **Total Power Consumption**: 50mW typ, 65mW max

### TEMPERATURE RANGE

- **Temperature Range**: 
  - 25°C to 85°C
  - 25°C to 85°C

### ASSEMBLY INSTRUCTIONS

**CAUTION**: This module is not an embedded assembly and is not hermetically sealed. Do not subject to shock or water wash procedures that would allow direct contact with free liquids or vapors. Entry of contaminants may occur, causing performance degradation and permanent damage. Inspect after any assembly process and clean by hand.

### NOTES

- Specifications given in DAS1157
- Assumed to be linear, input 10V peak-to-peak
- Specifications subject to change without notice.
OPERATION
For operation, the only connections necessary to the DAS1157/DAS1158/DAS1159 are the ±15V and ±5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Analog input and digital output programming are user selectable via external jumper connections.

Input voltage ranges are selectable via user pin programming: 0 to +5V, 0 to +10V, ±5V and ±10V. Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement (DAS1157 and DAS1158). DAS1159 unipolar coding is provided in a modified binary format (MSB complement) while bipolar coding is two's complement only.

ANALOG INPUT SECTION
The analog input can be applied to just the A/D converter or to the internal sample/hold amplifier ahead of the A/D converter. When using just the A/D converter, apply the analog input per the voltage range pin programming shown in Table 1. When using the sample/hold amplifier in conjunction with a D/A converter, apply the analog input to the S/H INPUT terminal and connect the S/H OUTPUT terminal to the appropriate A/D converter analog input.

<table>
<thead>
<tr>
<th>Analog Voltage Input Range</th>
<th>Connect V IN or S/H Out To</th>
<th>Connect Analog Common To</th>
<th>Connect Ref Out To</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to +5V</td>
<td>ANAIN 1, ANAIN 2, ANAIN 3</td>
<td>Ground</td>
<td>NC*</td>
</tr>
<tr>
<td>0 to +10V</td>
<td>ANAIN 2, ANAIN 3</td>
<td>Ground</td>
<td>NC*</td>
</tr>
<tr>
<td>±5V</td>
<td>ANAIN 1</td>
<td>Ground, ANAIN 3</td>
<td>ANAIN 2</td>
</tr>
<tr>
<td>±10V</td>
<td>ANAIN 3</td>
<td>Ground, ANAIN 3</td>
<td>ANAIN 2</td>
</tr>
</tbody>
</table>

*No Connection

Table 1: Analog Input Pin Programming

Errors due to source loading are eliminated since the sample/hold amplifier is a high-impedance unity-gain amplifier. High feedthrough rejection is provided for either single-channel or multichannel applications. Feedthrough rejection can be optimized, in multichannel applications, by changing channels at the rising or falling edge of the S/H control pulse.

TIMING DIAGRAM
The timing diagram for the DAS1157/DAS1158/DAS1159 is illustrated in Figure 3. This figure also includes the sample/hold amplifier acquisition time.

If the sample/hold amplifier is required, the TRIGGER input and S/H CONTROL terminal can be tied together providing only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of 5μs to insure accuracy. If the sample/hold amplifier is not used, the trigger pulse needs to be 1μs (minimum) in length to satisfy the A/D converter trigger requirements. At the falling edge of the trigger pulse, the sample/hold amplifier is placed in the hold mode, all internal logic is reset and the A/D conversion begins. The conversion process can be retriggered at any time, including during conversion.

With this negative edge of the trigger pulse, the MSB is set high with the remaining digital outputs set to logic low state, and the end of conversion is set high and remains high through the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched high at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-/16-bit conversion taking 50μs maximum. At this time, the end of conversion line goes low signifying that the conversion is complete. For microprocessor bus applications, the digital output can now be applied to the data bus by enabling the tri-state buffers. For maximum data throughput, the digital output data should be read while the sample/hold amplifier is acquiring the new analog input signal.
GAIN AND OFFSET ADJUSTMENT
The DAS1157/DAS1158/DAS1159 contain internal gain and
offset adjustment potentiometers. Each potentiometer has ample
adjustment range so that gain and offset errors can be trimmed
to zero.

Offset calibration is not affected by changes in gain calibration,
and should be performed prior to gain calibration. Proper gain
and offset calibration requires great care and the use of extremely
sensitive and accurate reference instruments. The voltage standard
used as a signal source must be very stable and be capable of
being set to within ±1/10LSB of the desired value at any point
within its range.

OFFSET CALIBRATION
For a 0 to +10V unipolar range, set the input voltage precisely
to +350μV for the DAS1157, +153μV for the DAS1158 and
+76μV for the DAS1159. For a 0 to +5V unipolar range, set
the input to +153μV for the DAS1157, +76μV for the DAS1158
and +38μV for the DAS1159. Then adjust the zero potentiometer
until the converter is just on the verge of switching from
00.0000000000 to 00.1111111111 (DAS1157/DAS1158) or from
10.0000000000 to 10.1111111111 (DAS1159).

For the ±5V bipolar range, set the input voltage precisely to
+350μV for the DAS1157, +153μV for the DAS1158 and
+76μV for the DAS1159. For a ±10V bipolar range, set the
input voltage precisely to +610μV for the DAS1157, +305μV
for the DAS1158 and +153μV for the DAS1159. Adjust the zero
potentiometer until the offset binary coded units are just on
the verge of switching from 00.0000000000 to 00.1111111111
and the two’s complement coded units are just on the verge of
switching from 10.0000000000 to 10.1111111111.

GAIN CALIBRATION
Set the input voltage precisely to +9.99999V (DAS1157)/
+9.99999V (DAS1158)/9.99999V (DAS1159) for the 0 to
+10V units, +9.99999V (DAS1157)/+9.99999V (DAS1158)/
+9.99999V (DAS1159) for 0 to +5V units, +9.9999V
(DAS1157)/9.99999V (DAS1158)/9.99999V (DAS1159) for
±10V units, or +9.99999V (DAS1157)/+9.99999V (DAS1158)/
+9.99999V (DAS1159) for ±5V units. Note that these values
are 1/2LSB less than nominal full scale. Adjust the gain
potentiometer until binary and offset binary coded units are just on
the verge of switching from 11.10 to 11.11 or modified binary
and two’s complement coded units are just on the verge of
switching from 01.10 to 01.11.

DAS1157/DAS1158/DAS1159 INPUT/OUTPUT
RELATIONSHIPS
The DAS1157/DAS1158 produces a true binary coded output
when configured as a unipolar device. Configured as a bipolar
device, it can produce either offset binary or two's complement
output codes. The most significant bit (MSB) is used to obtain
the binary and offset binary codes while (MSB) is used to obtain
two's complement coding. The DAS1159 produces a modified
binary coded output when configured as a unipolar device.
Configured as a bipolar device it can only produce two's
complement output codes. The DAS1159 uses MSB to obtain
the modified binary and two's complement output codes; the DAS1159
does not have an MSB output. Table II shows the DAS1157/
DAS1158/DAS1159 unipolar analog input/digital output
relationships. Table III shows the DAS1157/DAS1158/DAS1159
bipolar analog input/digital output relationships.

Input Voltage – Output Code Relationships

<table>
<thead>
<tr>
<th>Input Voltage</th>
<th>Unipolar Input Voltages</th>
<th>Digital Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to +5V Range</td>
<td>0 to +10V Range</td>
<td>Binary Code</td>
</tr>
<tr>
<td>DAS1157</td>
<td>+9.9997V</td>
<td>+9.997V</td>
</tr>
<tr>
<td>DAS1158</td>
<td>+5.0000V</td>
<td>+0.0000V</td>
</tr>
<tr>
<td>DAS1159</td>
<td>+5.0000V</td>
<td>+0.0000V</td>
</tr>
</tbody>
</table>

Table III. Bipolar Input-Output Relationships

<table>
<thead>
<tr>
<th>Analog Input</th>
<th>Bipolar Input Voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td>±5V Range</td>
<td>±10V Range</td>
</tr>
<tr>
<td>DAS1157</td>
<td>+9.9999V</td>
</tr>
<tr>
<td>DAS1158</td>
<td>+5.0000V</td>
</tr>
<tr>
<td>DAS1159</td>
<td>+5.0000V</td>
</tr>
</tbody>
</table>

Figure 4. Typical Ground Layout for DAS1157/DAS1158/
DAS1159